

**Remarks**

The instant Office Action dated April 2, 2009, notes the following new grounds of rejection: claims 8, 10-11 and 13 stand rejected under 35 U.S.C. § 112(2); claims 1, 3, 5, 7-8, 10-11 and 13 stand rejected under 35 U.S.C. § 103(a) over Chang (U.S. Patent No. 5,991,204) in view of Sharma (U.S. Patent 5,488,579) and further in view of a Quirk reference (“Semiconductor Manufacturing Technology”); claims 4 and 14 stand rejected under 35 U.S.C. § 103(a) over the ‘204, ‘579 and Quirk references and further in view of Hong (U.S. Patent No. 5,614,746); and claim 6 stands rejected under 35 U.S.C. § 103(a) over the ‘204, ‘579 and Quirk references and further in view of Chen (U.S. Patent No. 6,091,104). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

All rejections under § 103 are improper because the newly-cited “Quirk” reference is undated. As such, Applicant has no manner in which to evaluate whether the reference is prior art. Should any rejection be maintained, Applicant submits that the finality of the instant Office Action must be removed, and further that the Examiner must address Applicant’s traversals as presented herein (and in the record as applicable to the previously-cited references).

Applicant further submits that the § 103 rejections are improper because the Examiner has impermissibly ignored Applicant’s traversals regarding the combination of the ‘204 and ‘579 references, upon which every rejection relies. While the undated “Quirk” reference has been added, this reference does not address the majority of Applicant’s traversals, which remain applicable to the asserted combination of the ‘204 and ‘579 references. Therefore, Applicant’s traversals are not “moot” as asserted, and the Examiner’s failure to address these traversals is further contrary to M.P.E.P. §707.07(f) and applicable law. Applicant thus fully incorporates its traversals of record herein, which establish in the (uncontroverted) record that the cited combination of references does not teach or suggest the claim limitations. The following discussion further highlights the lack of correspondence between the cited combinations of references and the claimed invention, and further addresses the § 112(2) rejections, which are either erroneous or no longer applicable.

All of the claim rejections are improper because the various cited references fail to teach or suggest all claim limitations, and further because the Office Action's attempt to combine unrelated teachings from different references to show correspondence to individual claim limitations fails to show correspondence to the claims as a whole. For example, the instant Office Action's addition of a dry etch as described in the undated Quirk reference misinterprets the Quirk reference and thus fails to show teaching or suggestion of claim limitations relating to using an anisotropic etch to remove material over a tunnel dielectric. The cited dry etch does not leave an underlying tunnel dielectric intact, and in fact completely removes the underlying tunnel dielectric. Referring to cited figure 16.29 on page 460, the gate dielectric has been completely removed in a region that is adjacent to the gate, in a process involving an anisotropic etch that does not involve using a tunnel dielectric to protect the underlying substrate, but is rather made to "avoid any microtrenching" underneath the gate (as cited in the Office Action). This is part of an overetching step that includes removing the dielectric, as consistent with the discussion following figure 16.29 and describing a "*breakthrough step* that removes the native oxide" (emphasis in original). This is contrary to (and thus fails to teach or suggest) claim limitations directed to using the tunnel dielectric to protect portions of the substrate adjacent to the gate, then subsequently removing the tunnel dielectric *after* the anisotropic dry etch has been used.

The § 103 rejection is also improper because the secondary '579 reference, as applicable to all claim rejections, is directed to an inverted gate structure having spacers that cannot and do not mitigate oxygen diffusion as claimed because they are not positioned to do so. Moreover, the cited inverted gate structure in the '579 reference is further unrelated to the (conventional) structure of the '204 reference and issues relating to the manufacture of the same. Due to this inverted structure, gate oxides 35 and 38 of the '579 reference are completely exposed during any subsequent oxide growth, relative to the spacers 37. The cited spacer 37 therefore does not and cannot be used to mitigate the diffusion of oxygen in an interlayer dielectric layer because such layers are formed over the spacer (e.g., tunnel oxide 38 is formed over and after the spacer 37, which thus cannot mitigate any diffusion as asserted). While nitride spacers may exhibit characteristics relative to the mitigation of oxygen diffusion, none of the cited references

teach or suggest limitations directed to “using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.” Accordingly, modifying the ‘204 reference with the nitride spacers 37 in the ‘579 reference stops far short of providing an enabling disclosure that teaches or suggest the spacers and/or diffusion mitigation as claimed in the instant invention. Despite Applicant’s traversals, the instant Office Action has ignored these issues, and nothing in the record has established teaching or suggestion of claim limitations directed to a control gate and a floating gate separated by an interlayer dielectric layer, and spacers configured and arranged to mitigate oxygen diffusion to the interlayer dielectric layer.

Applicant further submits that the § 103 rejections are improper because the cited references teach away from the claimed invention, and further because the Office Action’s alleged motivation for combining references is both unrelated to the proposed modification and fails to address issues with modifying the primary ‘204 reference as asserted. Regarding the teaching away, M.P.E.P. § 2143.01 explains the long-standing principle that a §103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main (‘983) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int’l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) (“[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.”). As described above, the Quirk reference teaches using an anisotropic etch to remove a dielectric layer. The asserted tunnel dielectric layer 104 in the ‘204 reference is also completely etched in the step used to etch the asserted first conductive layer (floating gate poly 103 in figure 6a). Accordingly, both the ‘204 and Quirk references teach removing the dielectric layer, and in the case of the undated Quirk reference, does so using an anisotropic etch. The alleged “selectivity” in the Quirk reference is only to those portions of the dielectric that are below the gate (see figure 16.29). Both of these references directly teach away from the claimed invention, which involves using an anisotropic etch to maintain an underlying tunnel dielectric layer.

Regarding the lack of motivation, the Office Action’s attempt at modifying the ‘204 reference without providing examples from the prior art in support of such modification is contrary to § 103 and relevant law (*see KSR Int’l Co. v. Teleflex, Inc.*,

cited above, requiring evidence of motivation where the primary reference is modified. In this instance, the alleged motivation to combine the undated Quirk reference with the ‘204 reference is to provide “high selectivity and low device damage” but is silent as to how these features would be applicable to the ‘204 reference or how the ‘204 reference could function as such. For example, while the Office Action provides no discussion whatsoever as to how the dry etch in the Quirk reference would be combined with the ‘204 reference, it appears that adding a dry etch to the ‘204 reference would be inapplicable because the asserted tunnel dielectric layer 104 is completely etched in the step used to etch the asserted first conductive layer (floating gate poly 103 in figure 6a). Moreover, the Quirk reference uses its anisotropic etch to remove the gate dielectric as discussed above, thus effectively teaching away from the claimed approach to leaving the tunnel dielectric intact.

In view of the above, the cited combination of references does not teach or suggest all limitations in the independent claims. Applicant therefore believes that the § 103 rejections are improper and should be removed.

Applicant respectfully traverses the § 112(2) rejection of claim 10 and declines to limit the claim as suggested in the Office Action. The § 112(2) rejection of claim 10 erroneously attempts to require the Applicant to limit the recited spacer to a previously-discussed spacer. While the recited spacer may include a previously-discussed spacer, the claim is not so limited. Nothing in §112(2) or applicable law would suggest that the claims be limited to only a single interpretation. At present, claim 10 is directed to various embodiments which may or may not include one of the previously-discussed spacers as the newly-recited “a spacer.” Moreover, the use of the term “a spacer” instead of “the spacer” clearly reflects that the spacer is not necessarily referring to or otherwise limited by a previously-discussed spacer.

Applicant also traverses the §112(2) rejection of claims 8 and 11 because the rejection is effectively based upon an assertion that claim limitations directed to a “floating gate dielectric” be limited to word-for-word correspondence with the specification, which is contrary to the M.P.E.P. and relevant law. Moreover, Applicant believes that the term “floating gate dielectric” meets all requirements under §112(2), in that anyone of skill in the art would unmistakably understand its placement as defined

“on a substrate” with a floating gate “on the floating gate dielectric.” Moreover, this is also consistent with other claims that refer to the sidewall dielectric that the Examiner refers to as a “sidewall floating gate dielectric,” leaving no room for confusion.

Notwithstanding this, Applicant has amended claims 8 and 11 to remove the term “floating” in an effort to appease the Examiner. Applicant believes that this amendment does not change the scope of the claims or narrow the claims, and is further believes that the amendment is unnecessary for patentability. A similar amendment has been made to claims 10 and 13 for consistency.

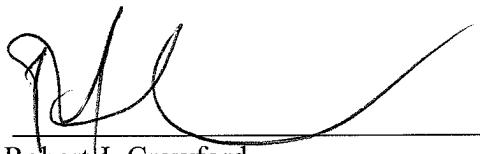
Applicant traverses the §112(2) rejections of claims 10 and 13 because the rejection is based upon erroneous assertions that the recited positional limitations relative to a wet-etched gate dielectric are process limitations, that the resulting gate dielectric cannot be defined by a wet etch, and further that the wet-etched gate dielectric “does not exist.” Regarding the alleged “process” limitations “a wet-etched portion of the floating gate dielectric,” these limitations identify a particular portion of the gate dielectric that is used to identify a relative position of the substrate (*i.e.*, the Examiner left off part of the limitation, which recites “an access gate dielectric on the substrate immediately adjacent to a wet-etched portion of the floating gate dielectric”). Regarding structural limitations, the resulting floating gate dielectric may include characteristics defined by such a wet-etching and, as such, these limitations would apply as structural characteristics defining the gate dielectric. The Office Action’s further assertion that the wet-etched portion of the gate dielectric “does not exist” is also erroneous because, while the wet-etching removes a portion of the gate dielectric, a portion of the gate dielectric that has been wet-etched (*i.e.*, at its exposed surface) remains. This is clearly exemplified in FIG. 9, with a portion of the wet-etched tunnel dielectric 51 remaining below the floating gate and against which an access gate dielectric 101 is formed. This further exemplifies the aforesaid positional relationship, the subject of which has nothing to do with “process” limitations as suggested in the Office Action.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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